VSS506

1.4MHz, 40V, 6A Synchronous Step-Down Regulator

General Description

The VSS506 is a high efficiency, synchronous step down regulator delivering up to 6A of output current making it ideal for medium load applications. It is designed to operate with wide input voltage range of 4.5 to 40V while maintaining very low supply current at no load. The output voltage is set via two external resistors to as low as 0.8V.

The device offers a multi-purpose MODE select pin allows selection between fixed frequency PWM and power save mode. When connected to logic high, the regulator is optimized for maximum efficiency over a wide range of load current. During full load operation, it operates in 700KHz of constant frequency. As the load reduces, the converter automatically transitions in to power save (P_{SVE}) mode maintaining high light load efficiency. The power save mode (P_{SVE}) entry point is set via external resistor optimizing the product for peak efficiency performance. For noise sensitive applications, the device can be forced to in to PWM mode by pulling MODE to logic low. In PWM mode, the device operates at fixed 700KHz switching frequency ensuring low output ripple across the entire load.

A SYNC/F_{SET} pin enabling external clock synchronization or programmable oscillator frequency. Connecting a resistor from this pin to GND sets the frequency from 0.5 to 1.4MHz. Applying a clock to this pin allows external clock synchronization. When connected to logic high, the regulator defaults to the internal clock.

The low resistance on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solution.

The output voltage startup ramp is programmed via external capacitor from SS pin to GND limiting the in rush current during startup. This feature allows operation as a standalone power supply or power sequencing. The regulator offers output short-circuit and thermal protection to safeguard the device under extreme operating conditions. An open drain power good output indicates when the regulator output is within ±5% of its nominal output. An enable pin provides on/off control of the regulator. When connected to logic low, the device enters shutdown and consumes less than 1µA of current.

The VSS506 is available in the QFN4X4-24 package, and it is rated for -40 to +85°C temperature range.

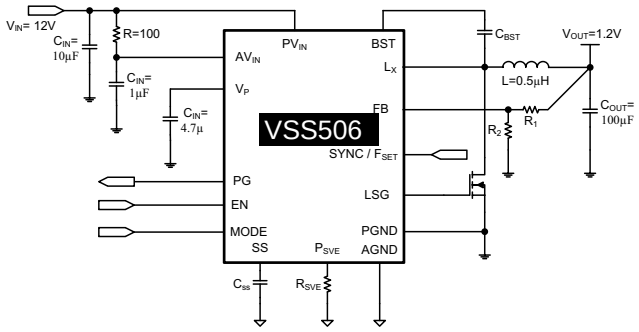
Features

- V_{IN} range: 4.5 – 40V
- Adjustable V_{OUT} as low as 0.8V
- 6A maximum output current
- Programmable switching frequency 0.5 – 1.4MHz
- MODE select pin
- Synchronizable to external clock
- Over-voltage protection
- Excellent line and load regulation
- Power good signal
- Programmable Soft-Start
- 50ns minimum on time
- Cycle-cycle & Hiccup Mode Current limit protection
- Thermal shutdown protection
- -40°C to +85°C temperature range
- Available in QFN4X4-24 package
- RoHS & WEEE compliant

Applications

- Telecommunication
- Servers
- Switches & Routers
- Notebook & desktop
- High current point of load

Typical Application



Pin Description

Pin #	Symbol	Description
	AV_{IN}	Analog supply for the internal circuitry. Connect a resistor and capacitor combination between this pin and ground. Refer to application section.
	PV_{IN}	Input supply Voltage for the converter power stage. Connect a 10µF capacitor from this node to ground.
	V_P	Internal 5V power supply. Connect a 4.7µF capacitor from this pin to GND.
	BST	Supply pin to the power transistor driver. Connect a 4.7µF capacitor between BST and L_X to supply the floating circuitry.
	PG	Power good. Open drain output. A logic low indicates the output voltage is less than desired value.
	FB	Feedback pin. Connect FB pin to the center tap of the resistor divider network.
	EN	Enable pin. A logic high forces the device to normal operation. When connected to logic low, the device shuts down and it draws less than 1µA of current.
	PGND / AGND	Power ground & analog ground connection.
	MODE	MODE select input pin. When connected to logic low, the device operates in fixed PWM mode. When connected to V_P, it is forced in both PSAVE/PWM mode.
	SS	Programmable soft start pin. Connect a capacitor from this pin to ground to set the output voltage ramp time. Floating this pin will default to internal soft start.
	P_{SAV}	Connect a resistor from this pin to ground to program the entry point for the power save mode when MODE pin is connected to logic high.
	SYNC / F_{SET}	Apply an external clock signal for external frequency synchronization. Connecting an external resistor from this pin to ground sets the oscillator frequency. A logic high defaults to internal clock.
	LSG	Low Side Gate driver. Connect a external MOSFET for proper operation.

Pin Configuration (TBD)

QFN4X4-24 (Top View)

Table 1: MODE Select

MODE	Function
GND	PWM (fixed frequency) Mode
High	PWM/PSave

Table 1: Oscillator frequency Selection

SYNC/F_{SET}	Function
Logic High	Internal oscillator (700KHz)
Resistor to GND	Programmable oscillator (0.5–1.4MHz)
Clock	Synchronized to external clock

Absolute Maximum Ratings (1)

Maximum Input Supply Voltage ..... -0.6V to 42V
Enable Voltage ..... -0.6V to 42V
MODE, Power good (PG), SYNC, SS, P_{SAVE} Voltage ..... -0.6V to 6.0V
Boost pin (BST) Voltage ..... -0.6V to 42V
Switch node Voltage ..... -0.6V to 42V
Feedback Voltage (FB) ..... -0.6V to 6.0V

Recommended Operating Conditions

Input Voltage ..... 4.5 to 40V
Ambient Operating Temperature ..... -40°C to +85°C

Thermal Information (2)

QFN4X4-24 θ_{JA} ..... 35˚C/W
Storage Temperature Range ..... -65 to 150˚C
Lead Temperature (soldering 10s) ..... 260˚C
Junction Temperature ..... -40°C to +125°C

Electrical Characteristics

UNLESS OTHERWISE NOTED:

V_{IN}=12V; V_{OUT}=1.2V;C_{IN}=10µF; C_{OUT}=100µF;L=1.5µH; -40˚C≤T_A=T_J≤85˚C; $T_{J(MAX.)}$= 125°C; TYPICAL VALUES ARE T_A= 25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Under voltage Lockout	UVLO			3.5		V
Feedback Voltage	V_{FB}	Adjustable V_{OUT} only	TBD	0.8	TBD	V
Feedback bias current	I_{FB_Bias}	Adjustable V_{OUT} only		10	100	nA
Maximum Output Current	I_{OUT_Max}		6.0			A
Load Regulation		I_{OUT}= 10mA – 6A	-1.5		1.5	%
Line Regulation		V_{IN}=4.5 – 40; I_{OUT}=10mA	-0.5		0.5	%
Supply Current	I_{SUP}	No load; MODE=V_P		5.0		mA
		No load; MODE=GND		1.2		mA
Shutdown Current	I_{SHDN}	V_{EN}= 0V			1.0	µA
Current Limit[2]	I_{LIM}		10	9.0		A
Oscillator Frequency	$F_{OSC.}$	SYNC/F_{SET}=V_P		0.7		MHz
		Resistor from SYNC/F_{SET} to GND	0.5		1.4	
Synchronizable Frequency Range	F_{SYNC}	50% duty cycle	0.5		1.4	MHz
Soft start charging current	T_{SS}	V_{SS}=0.8V	0.8	1.0	1.2	µA
Power good low threshold	V_{PG}		90			%
Power good high threshold	V_{PG}				95	%
Power Good Leakage current	I_{PG}	PG off; V_{PG}= 12V		0.01		µA
High Side Switch Resistance	R_{DSON_P}	I_{OUT}= 5A		30		mΩ
Low side gate driver sink current				1.5		A

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Low side gate driver source current				1.5		A
Minimum Duty Cycle	D_{MIN}		7.0	3.5		%
Maximum Duty Cycle	D_{MAX}				95	%
Input Low Voltage Threshold	$V_{EN(L)}$			1.0	1.7	V
Enable High Voltage Threshold	$V_{EN(H)}$		2.0	1.8		V
Input Low Current	$I_{EN(L)}$	V_{EN} = 0V	-1.0		1.0	µA
Input High Current	$I_{EN(H)}$	V_{EN} = V_{IN}	-1.0		1.0	µA
Thermal Shutdown	T_{SD}			140		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			10		°C

Notes:

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.
2. Measured on approximately 1” square of 1oz copper
3. The VSS506 is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range and is assured by design, characterization, and correlation with statistical process control.
4. Load regulation is measured using pulse techniques with duty cycle <5%.

Application Hints

Input Capacitor (C_{IN})

The VSS506 has two separate input supplies powering the regulator. The PV_{IN} is used to power the high side switch of the output power stage, and AV_{IN} is used for the rest of the circuit. Since PV_{IN} provides the entire load current each time the switch turns on, it contains all the switching noise. A bulk 10µF capacitor from PV_{IN} to ground is recommended.

The AV_{IN} pin powers the internal analog circuitry of the regulator. It is important to minimize the switching frequency ripple from PV_{IN} to this pin. A combination of 100Ω resistor and 1µF capacitor from this pin to ground is recommended. Refer to the figure below:

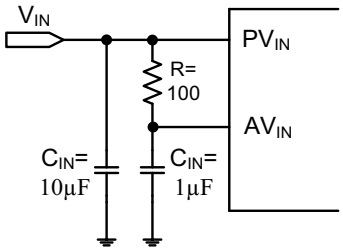


Figure 1: Filtering power supply

For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline.

Placement of the capacitor is critical for good high frequency noise rejection. See layout guidelines section for details. Switching frequency ripple is also filtered by ceramic bypass input capacitor.

Output Capacitor (C_{OUT})

The output capacitor is not only used to filter out the inductor current, but also, enhances the load transient response. The inductor current filtering requirement is a function of the switching frequency and the magnitude of the ripple current. The load transient requirement is a function of the slew rate (di/dt) and the magnitude of load current step. These requirements are generally met with a mix of capacitors and careful layout.

Since VSS506 is internally compensated, a 100µF ceramic capacitor in conjunction with a 1.5µH inductor is sufficient for stability and filtering the ripple current. Use only bulk, low-ESR capacitors intended for switching-regulator applications. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications.

Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden, AVX, and Murata.

Inductor Selection (C_{OUT})

The inductor selection is critical to the performance of the VSS506. The inductor affects stability, transient response, and efficiency. A good compromise between physical size, transient response, and efficiency is achieved when we set the inductor ripple current ratio between 0.2 and 0.4.

Once the appropriate value is determined, the component is selected based on the DC current and the peak (saturation) current. Select an inductor that has a DC current rating greater than the full load current of the application. The DC current rating is also reflected in the DC resistance (DCR) specification of the inductor. The inductor DCR should limit the inductor loss to less than 2% of the step down converter output power.

MODE Select & P_{SVE}

The MODE pin allows selecting the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

To optimize the power save entry and efficiency, the VSS506 offers a programmable power save mode by connecting a resistor from this pin to ground. The resistor value is selected as follows:

$$R_{SET} = \frac{20K}{I_{PK-Ripple}}$$

Peak ripple current ($I_{PK-Ripple}$) is load current+ inductor ripple current divided by 2. Connecting P_{SVE} to logic high forces the regulator to a default point.

The regualtor can be forced in to fix switching frequency by connecting MODE select pin to logic low. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the light load efficiency is lower compared to the power-save mode.

Power Good

The power good output can be used for sequencing purposes. Enabling a separate regulator once the output voltage is reached, or to indicate that the output voltage is in regulation. When the device is disabled, the PG pin is pulled high by the internal open-drain output transistor.

Internally, the VSS506 compares the feedback voltage FB to the nominal reference voltage of typically 0.8 V. If the feedback voltage is more than 95% of this value then the power good output is low impedance. If the feedback voltage is less than 90% of the reference voltage then PG pin is pulled high.

Output Voltage

The adjustable output voltage allows the user to program the output voltage by using an external resistor divider.

VSS506 uses a 0.8V reference voltage at the positive terminal of the error amplifier. To set the voltage, a programming resistor from the feedback pin (FB) to ground must be selected. A 10kΩ resistor is a good selection for a programming resistor R2 (see figure 2). A higher value may result in an excessively sensitive feedback node while a lower value will draw more current and degrade the light load efficiency. The equation for selecting the voltage specific resistor is:

$$V_O = \left(1 + \frac{R1}{R2}\right) * V_{FB}$$

The table below provides the resistor values for some common voltages.

R2	R1	V_{OUT}
10KΩ	52.5KΩ	5.0V
10KΩ	31.3KΩ	3.3V
10KΩ	21.3KΩ	2.5V
10KΩ	12.5KΩ	1.8V
10KΩ	8.8KΩ	1.5V
10KΩ	5.0KΩ	1.2V

Table 1: Feedback Resistor Values

Enable

The enable pin provides electrical on/off of the regulator. To assure the regulators will switch on; the EN must be greater than 2.0 volts. The device will shut down when the voltage on the EN pin falls below 1.7 volts. In shutdown, the regulator will consume low current. If the enable function is not needed in a specific application, it may be tied to Vin to keep the device in a continuously on state.

Programmable Soft Start

A capacitor (Css) from SS pin to ground sets the start time. The soft start capacitor is charged with a 1 microampere current that charges the external slow start capacitor.

$$C_{SS} = T_{SS} * 8E5$$

The regulator will default to the internal 500μS if the SS pin is left floating.

Frequency Selection / Synchronizable to external clock

The SYNC/F_{SET} is a multi-function pin. Connecting it to logic high, the converter operates with a typical switching frequency of 700KHz.

It is possible to synchronize the converter to an external clock within a frequency range from 500KHz to 1400KHz. The device automatically detects the rising edge of the first clock and is synchronizes immediately to the external clock. For proper operation, a 50% duty cycle is highly recommended.

Connecting a resistor from SYNC/F_{SET} programs the regulators switching frequency from 500KHz to 1400KHz. The frequency is set by:

$$R_{SET} = \frac{8.6E10}{Frequency}$$

The frequency tolerance is ±20%.

Thermal shutdown

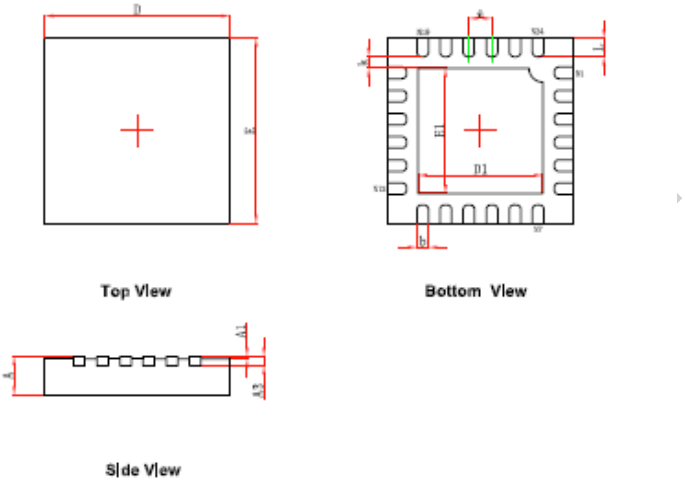
The VSS506 has an internal thermal protection circuit that will turn on when the device die temperature exceeds 145°C. The internal thermal protection circuit will actively turn off the high side output device to prevent the possibility of over temperature damage.

The regulator output will remain in a shutdown state until the internal die temperature falls back below the 145°C trip point.

Ordering Information

Device	Package	Output Voltage	Packing Method & Quantity
VSS506QFN4424	QFN4X4-24	Adjustable	2500 Tape & Reel

Outline Drawing and Landing Pattern – QFN4X4-24



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020